

Register Description and Programming Requirements Printer Personality

Warp Nine Engineering F/Port ISA Card

Revised 16 May 1995

Current Personality: PRINTERE

Summary

This document describes the register set and programming information for the PRINTER personality for the FarPoint Communications' F/Port card (P/N 510-0002). For additional information, see the FarPoint Document, "*F/Port Register and Programming Examples*".

The logic for this card is implemented using the Xilinx 2064 Field Programmable Gate Array. The FPGA allows us to have multiple design 'personalities' for use with one card. The hardware configuration of the card can be modified in real time on a powered PC without the need to reboot or change any external jumper settings.

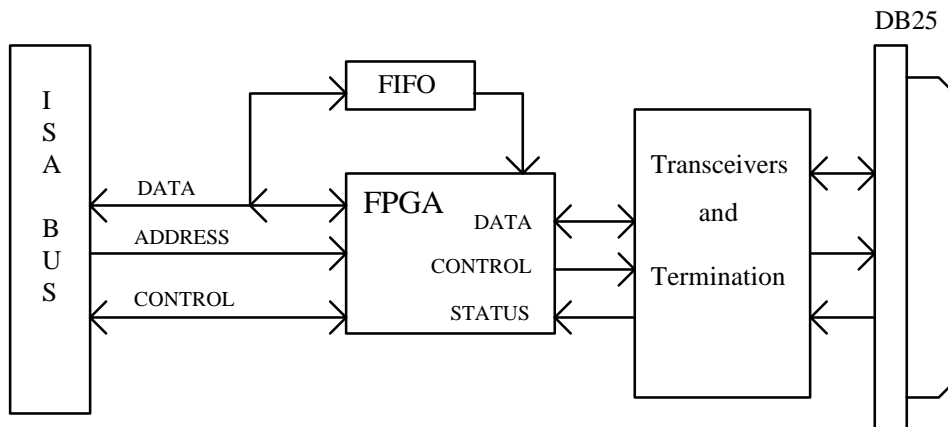
The printer personality, PRINTER_x (x denotes Rev level), defines the F/Port hardware to look like a high performance "Centronics" style printer input port. The main features of the port are:

- 512 Byte input FIFO
- Greater than 1Mb per second input data burst rate
- Autostrobing with host interface
- Supports 8 bit Byte mode for reverse channel data transfer (software assisted)

This document will describe the register definitions and then programming criteria for the card.

Block Diagram

The F/Port card is essentially a FIFO and Xilinx FPGA with an ISA interface and a DB25 with transceivers and termination. The following diagram illustrates the architecture:



Please Note: Because the FIFO's input data port and the PC data are on the same bus, there are some architectural limitations to the type of operations that can be performed with this configuration. These will be highlighted.

I/O Map and IRQ

The F/Port card uses 8 contiguous I/O registers beginning at one of four starting locations:

278	LPT2
280	General I/O
290	General I/O
378	LPT1

The base address is jumper selectable.

The interrupt, IRQ, level is jumper selectable. The options are:

5 7 10 11 12 15

The card may be inserted in either an 8 bit or 16 bit I/O slot. If used in an 8 bit slot then only IRQ levels 5 or 7 may be selected.

Configuring the F/Port Card

To configure the F/Port card with the PRINTERx personality, use the FPCONFIG program:

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FPCONFIG -dPRINTERX -p<port>
```

ie:

```
FPCONFIG -dPRINTERE -p290
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will download the PRINTERE personality to a F/Port installed at address 290.

PORT Definitions

The following table defines the ports for the PRINTERx mode:

Base Offset	R/W	PRINTER Mode	Notes
0	R/W	Reverse Channel data port	
1	R/W	Printer control/status port	read/write have different bit meanings
2	R	FIFO data port 0	Used for 8 or 16 bit I/O
3	R	FIFO data port 1	Used for 2nd byte in 16 bit I/O
4	W	Mode/Config Register	
5	R	Printer STOP register	READ ONLY-
6	R	Printer START register	READ ONLY-
7 (1)	W	FPGA config register	Do not use

(1) This port is used to reset and configure the FPGA. This port should never be written to.

Register Definitions

The following tables define the bits used by the various registers. All signals are asserted true unless defined as "nXXX" which implies that signal 'XXX' is asserted low when its corresponding bit is written as a logic 1. On registers that are read only, 'nXXX' implies that the signal condition is true when read low.

Port 0-Reverse Channel Data Port

Bit	Read/Write
<0:7>	I/O Data

Port 1-Printer Control/Status Port

Bit	Write	Read
0	IRQ_EN	IRQ_EN
1	SET_ACK	nFIFO_EMPTY
2	SET_BUSY	BUSY
3	SET_FRST	nFIFO_FULL
4	PE	nAUTOFEED
5	ERROR	nSTROBE
6	SELECT	nSELECTIN
7	EN_PORT_WR	nINIT ⁽¹⁾

(1) Prior to “PRINTERD” personality this was a read back of EN_PORT_WR

Write

IRQ_EN Enables F/Port interrupt on FIFO_FULL when set to 1. Default 0
 SET_ACK Asserts printer port ACK line low when set to 1. Overrides state machine ACK line. Default 0

- SET_BUSY Asserts printer port BUSY line high when set to 1. Overrides state machine BUSY line. Default 0
- SET_FRST Drives the reset pin of the FIFO memory. To reset FIFO, set to 1 then 0. Input line, nINIT, will reset the FIFO. Default 0.
- PE When asserted, sets the printer port PE line to 1. Default 0
- ERROR When asserted, sets the printer port ERROR line to 1. Default 0
- SELECT When asserted, sets the printer port SELECT line to 1. Must be set to enable the printer state machine. Default 0
- EN_PORT_WR When asserted, sets the printer data port to the out direction. Data written to the Reverse Channel data port (0) is presented onto the printer ports data lines. The printer must be stopped to use this feature. Defaults 0

Read

- IRQ_EN Readback of the control port bit 0.
- nFIFO_EMPTY FIFO empty status bit. When 0, the FIFO has no data
- BUSY Status of the printers interface BUSY line
- nFIFO_FULL FIFO full status bit. When 0, the FIFO is full with 512 bytes of data. This will remain asserted until at least one byte is read from the FIFO.
- nAUTOFEED Status of the printers interface nAUTOFEED line
- nSTROBE Status of the printers interface nSTROBE line
- nSELECTIN Status of the printers interface nSELECTIN line
- nINIT Status of the printers interface nINIT line. Prior to PRINTERD, this was a readback of EN_PORT_WR

Port 2- FIFO Data Port 0

Bit	Read
<0:7>	FIFO Data

8 bit or 16 bit data is read from this port.

Port 3- FIFO Data Port 1

Bit	Read
<0:7>	FIFO Data

When 16 bit I/O is used, this port provides the 2nd byte. This is transparent to the software and all I/O (8 or 16 bit) is done through the FIFO Data Port 0.

Port 4- Mode Register- Write Only

Bit	Write
0	AUTOMODE
<1:7>	Not Used

Write

AUTOMODE When set to 1, allows the printer state machine to be enabled. When 0, the printer state machine cannot be started, and the printer status lines will respond to the control register. In particular, the BUSY and the ACK line will be controlled by the control register values and will be independent of

printer state machine. Default is 0.

Port 5- Printer STOP Register

Reading from this port disables the printer port state machine and allows the software to read the data in the FIFO, the Status port or write to the Control port. If SELECT is asserted, then the BUSY line is driven high until either SELECT is deasserted or the state machine is enabled again via the Printer START register. This port should never be written to.

Port 6- Printer START Register

If the AUTOMODE bit is set to 1, then reading from this port enables the printer port state machine and allows for the automatic reception of data from the host platform. In order for the state machine to receive data the following criteria must be set:

- SELECT line asserted
- nSELECTIN asserted
- nINIT not asserted
- FIFO not full

If these criteria are met, then the state machine will do all the handshaking with the STROBE, BUSY and ACK line and transfer data from the port to the FIFO. When the FIFO is full (512 bytes received), the BUSY line will be asserted, and an Interrupt generated.

Port 7- Xilinx Configuration Port

Used to reset and configure the Xilinx FPGA. This port should never be accessed.

Writing Software Drivers for the Printer Personality

Writing a software interface for the Printer personality is rather straightforward. There are a few boundry conditions that will be discussed.

Enabling Printer Mode

When the Printer personality is first downloaded, the interface is in the quiescent idle state. The control register (R1) is reset to 0x00h (interrupts disabled, no SELECT) and the printer interface state machine is disabled.

To enable the card to accept host data, do the following:

- 1- First initialization of the port (one time only):
 - A) Poll Status port until nSELECTIN is asserted (R1 bit6=0)
 - B) Set the AUTOMODE enable bit (0x01h => R4)
 - C) Set SELECT and enable interrupts (0x41h => R1)
- 2- Enable state machine (this will be done for each packet):
 - A) Enable the Printer state machine (inbyte R6)
 - B) Start a background activity timer that will signal a check for last packet (50mS)

At this time, the card will accept data from the host until the FIFO is full (512 bytes). At that time the BUSY line will remain asserted and an interrupt will be generated. If this was the last packet and the amount of data was less than 512 bytes, then the background timer will probably generate an interrupt.

Reading Data from the FIFO- Interrupt Service Routine

There are two routines required to read data from the FIFO. The first deals with the FIFO full condition or the first n modulo 512 packets, and the second is the last packet (runt) ending condition where less than 512 bytes were transferred.

FIFO Full Routine

When the FIFO full interrupt is generated then do the following:

- 1- Stop background activity timer
- 2- Disable the Printer state machine (inbyte R5)
- 3- Read the FIFO data:
 - A) 512 inbyte from R2
 - B) 256 inword from R2
- 4- Re-enable the Printer state machine

Ending Condition- Background Activity Timer Routine

The assumption is that the timer is set to go off at a time that is much greater than the time necessary to transfer 512 bytes, and this is probably the end of the file.

- 1- Disable the Printer state machine (inbyte R5)
- 2- Read the Status port and check that the FIFO is not empty (R1 bit1=1)
- 3- If not empty then read a BYTE from the FIFO data port (inbyte R2)
Go back to 2 and repeat until the FIFO empty flag is set (R1 bit1=0)
- 4- Re-enable the Printer state machine

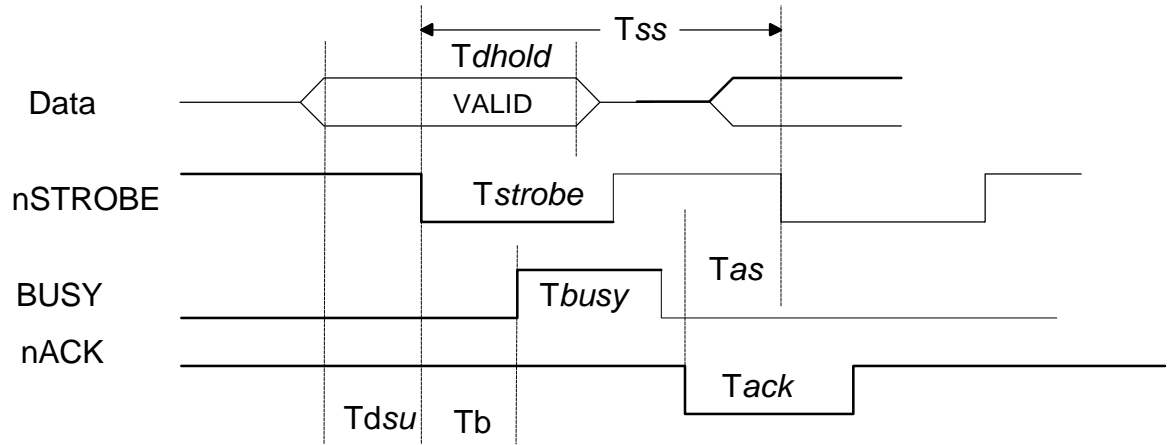
Miscellaneous Conditions

Printer error states such as PE and ERROR can be set on the printer interface by setting the appropriate bit in the Control/Status port (R1). In order to do this, you must first disable the printer state machine by reading from the Stop port (R5).

When the printer is disabled you can send reverse channel data by writing the data to the Reverse Data Port (R0) and then setting the data enable line (R1 bit7=1). Byte or Nibble mode data transferred is done via software generation and checking of the control and status lines.

Interface AC Timing Requirements

The following diagram indicates the critical timing parameters for this interface personality.



Parameter	Min (nS)	Max (nS)	Definition
<i>Tdsu</i>	0	N/A	Data setup to nSTROBE asserted
<i>Tb</i>	100	250	nSTROBE asserted until BUSY asserted
<i>Tstrobe</i>	300	1000	Strobe width
<i>Tbusy</i>	300	375	BUSY width
<i>Tdhold</i>	400	500	data hold from nSTROBE asserted
<i>Tas</i>	0	N/A	nACK asserted until next nSTROBE
<i>Tack</i>	400	500	nACK width
<i>Tss</i>	400	625	minimum Strobe to Strobe timing

Min and Max timings are dependant upon the ISA BUSCLOCK frequency. Min timings are based upon a 10Mhz Busclock (100nS/cyc) and Max timings are based upon an 8.0Mhz Busclock (125nS/cyc).